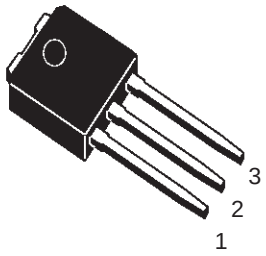
STD2NC40-1

N-CHANNEL 400V - 4.7Ω - 1.5A IPAK
PowerMesh™ II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD2NC40-1	400V	<5.5Ω	1.5A

- TYPICAL $R_{DS}(on)$ = 4.7Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

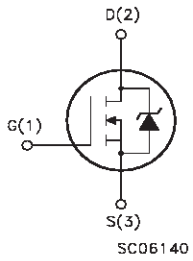


IPAK
(SUFFIX"-1")

DESCRIPTION

The PowerMESH™ II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns swithing speed, gate charge and ruggedness.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- SWITH MODE LOW POWER SUPPLIES (SMPS)
- CFL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuos) at T_C = 25°C	1.5	A
I_D	Drain Current (continuos) at T_C = 100°C	0.95	A
I_{DM} (•)	Drain Current (pulsed)	6	A
P_{TOT}	Total Dissipation at T_C = 25°C	30	W
	Derating Factor	0.24	W/°C
dv/dt	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	–60 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤1.5A, di/dt ≤100A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	4.16	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	1.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	275	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	1.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	125	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	400			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.7 A		4.7	5.5	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, V_{GS} = 10V	1.5			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D =0.7A		1.1		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		108		pF
C_{oss}	Output Capacitance			22.5		pF
C_{rss}	Reverse Transfer Capacitance			0.4		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 200V, I_D = 0.7A		7.5		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		12		ns
Q_g	Total Gate Charge	V_{DD} = 320V, ID = 1.5A, V_{GS} = 10V		6.1	8.2	nC
Q_{gs}	Gate-Source Charge			2.1		nC
Q_{gd}	Gate-Drain Charge			2.4		nC

SWITCHING OFF

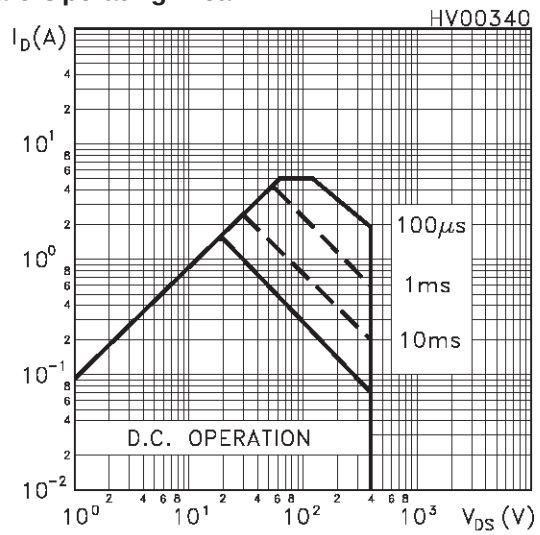
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 320V, I_D = 1.5A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		20		ns
t_f	Fall Time			27		ns
t_c	Cross-over Time			29		ns

SOURCE DRAIN DIODE

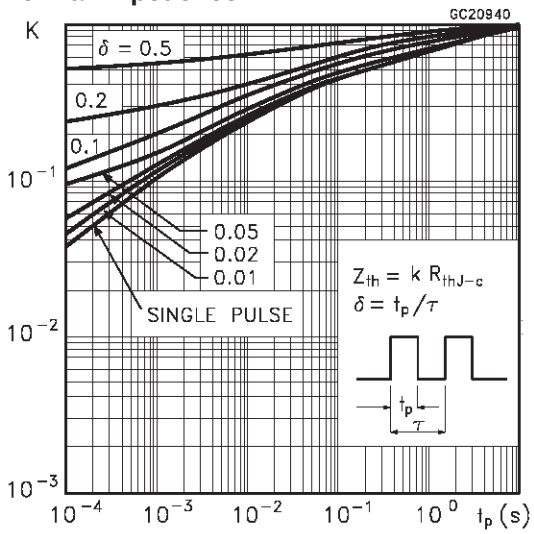
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				1.5	A
I_{SDM} (1)	Source-drain Current (pulsed)				6	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 1.5A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 1.5A, di/dt = 100A/µs, V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		180		ns
Q_{rr}	Reverse Recovery Charge			625		nC
I_{RRM}	Reverse Recovery Current			5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

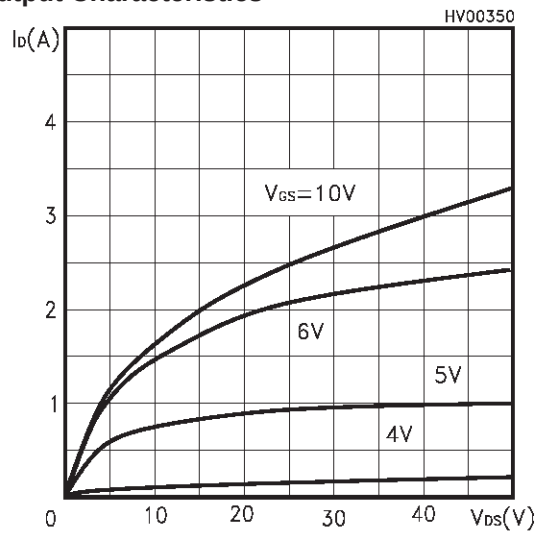
Safe Operating Area



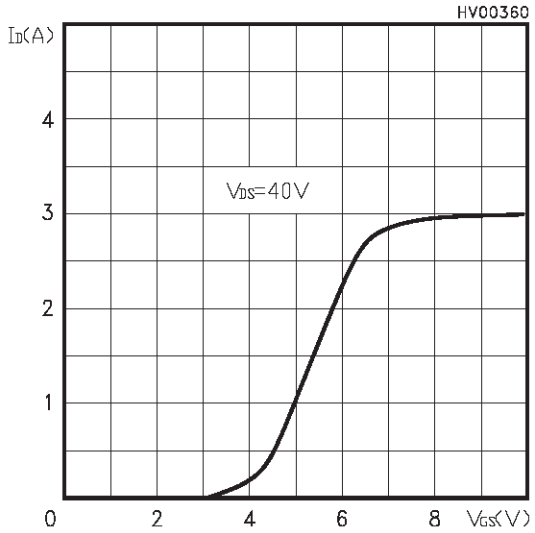
Thermal Impedence



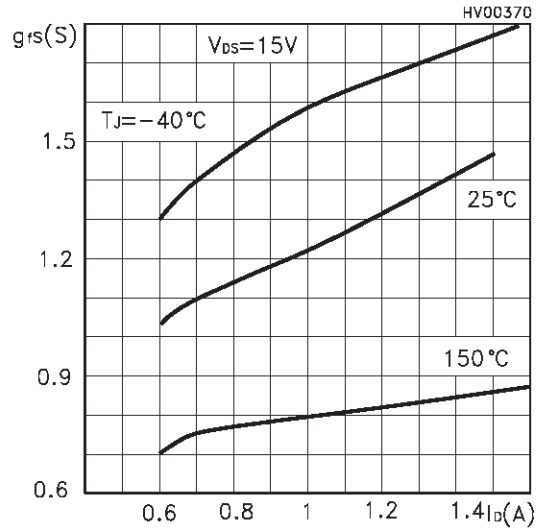
Output Characteristics



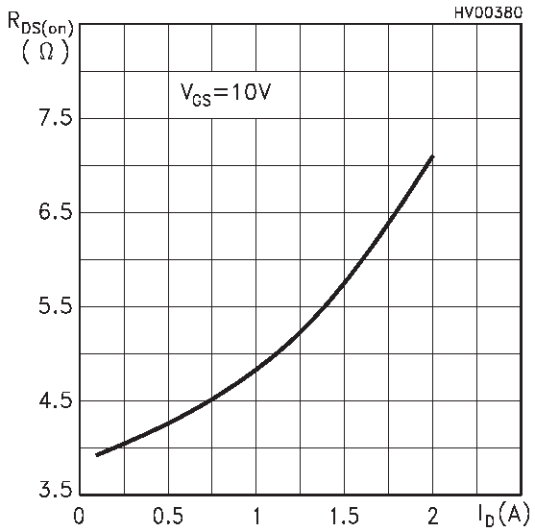
Transfer Characteristics



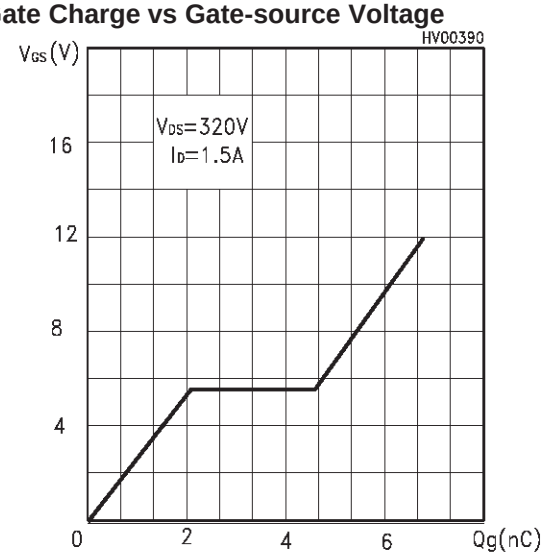
Transconductance



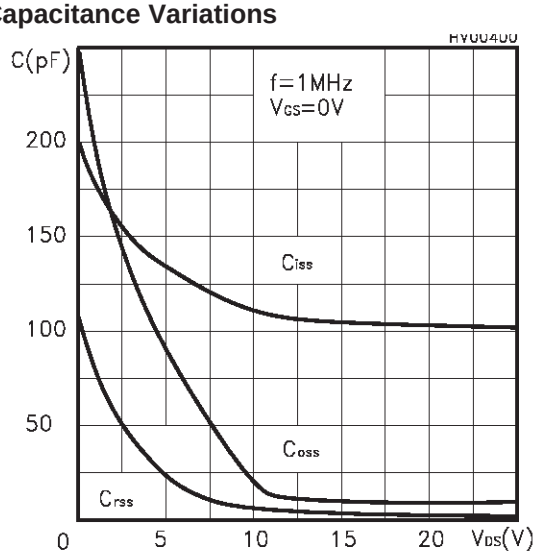
Static Drain-source On Resistance



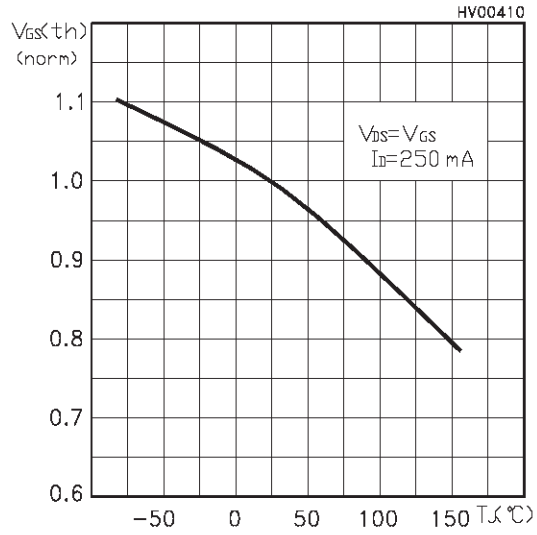
Gate Charge vs Gate-source Voltage



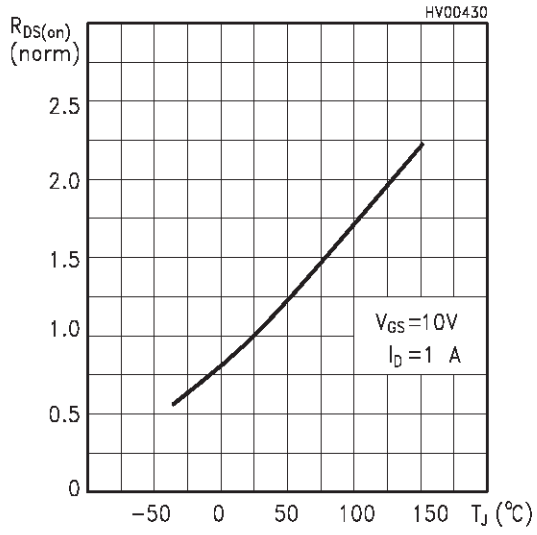
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

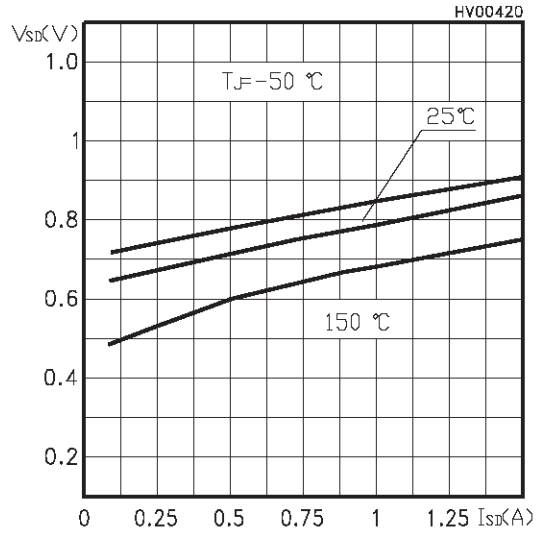


Fig. 1: Unclamped Inductive Load Test Circuit

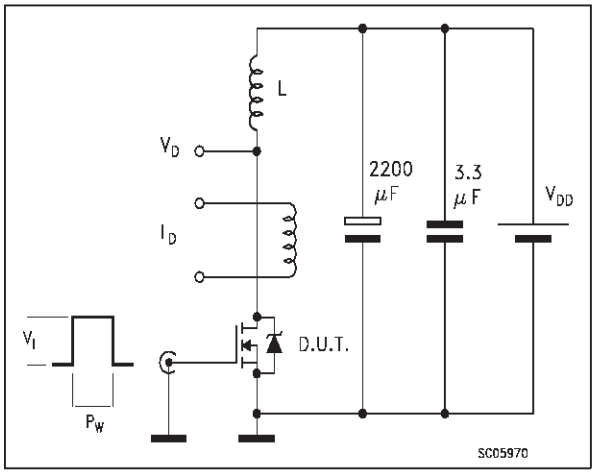


Fig. 2: Unclamped Inductive Waveform

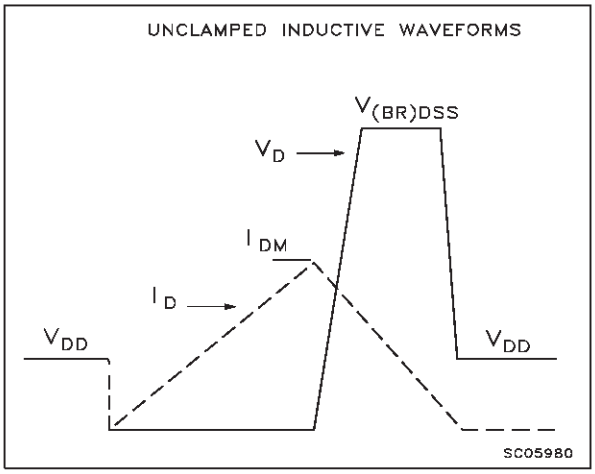


Fig. 3: Switching Times Test Circuit For Resistive Load

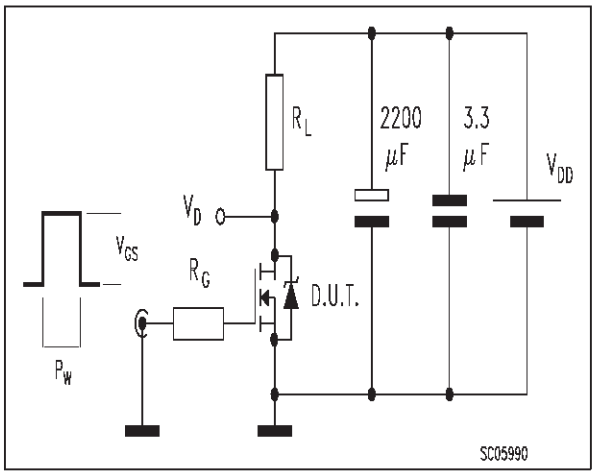


Fig. 4: Gate Charge test Circuit

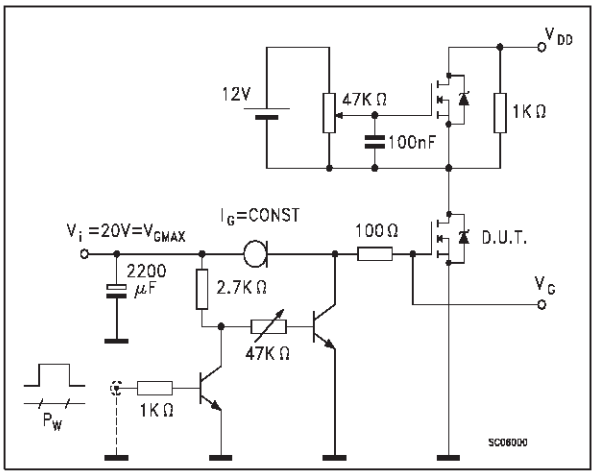
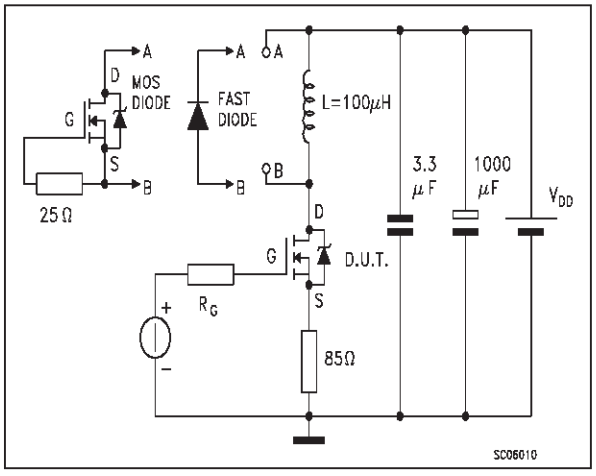
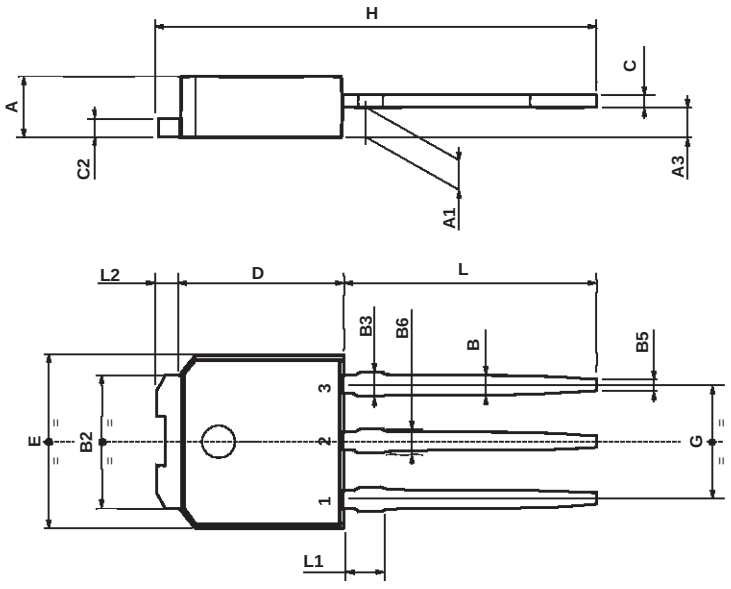


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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